

Application No. 10/622,614  
Amendment dated December 23, 2004  
Reply to Office Action of July 26, 2004

### **REMARKS**

#### **Objection To Title:**

**The title of the invention was objected to as allegedly not descriptive.**

The title has been amended to overcome the objection.

#### **Objection To Abstract:**

**The abstract was objected to due to informalities.**

The abstract has been amended to overcome the objection.

#### **Objection To Drawings:**

**The drawings were objected to under 37 CFR 1.83(a) because the drawings allegedly do not show every feature of the invention specified in the claims.**

It is respectfully submitted that every feature recited in the claims is shown in the drawings as explained below. The explanation is made only to show that every feature of the claims appears in the drawings, but should not be interpreted to limit the present invention to embodiments shown in the drawings.

Claim 1 is typically shown in FIGS. 4B and 6. The claim recitations correspond to the reference numerals as follows:

1. A semiconductor device comprising: a first insulating film (38, 40, 42) formed over a substrate (20); a first interconnection (58) buried in at least a surface side of the first

insulating film (38, 40, 42), the first interconnection (58) having a pattern which is bent at a right angle (see FIG. 4B); a second insulating film (62) formed on the first insulating film (38, 40, 42) with the first interconnection (58) buried in, and including a groove-shaped via-hole (66a) formed in a region above the first interconnection, the groove-shaped via-hole (66a) having a pattern which is formed along the pattern of the first interconnection (58) and is bent at a right angle (see FIG. 4B); and a first buried conductor (72a) filled in the groove-shaped via hole (66a).

Claim 8 is typically shown in FIGS. 4B and 5. The claim recitations correspond to the reference numerals as follows:

8. A semiconductor device according to claim 1, further comprising: a second buried conductor (72) buried in a hole-shaped via-hole (66) formed in the second insulating film (62) on the first interconnection (58).

Claims 10 and 12 are typically shown in FIGS. 4A and 4B. The claim recitations correspond to the reference numerals as follows:

10. A semiconductor device according to claim 8, wherein a width of the groove-shaped via-hole (66A) is 20 - 140% of a width of the hole-shaped via-hole (66) .

12. A semiconductor device according to claim 8, wherein a width of the groove-shaped via-hole (66A) is not more than a width of the hole-shaped via-hole (66).

Claim 22 is typically shown in FIGs. 4B, 6, 31 and 32. The claim recitations correspond to the reference numerals as follows:

22. A semiconductor device comprising: a conducting layer (106 or 206) buried in a surface side of a substrate (100 or 200), the conducting layer (106 or 206) having a pattern which is bent at a right angle (see FIG. 4B); an insulating film (108 or 208) formed on the substrate (100 or 200) with the conducting layer (106 or 206) buried in, and including a groove-shaped via-hole formed in a region above the conducting layer (106 or 206), the via-hole having a pattern which is formed along an extending direction of the conducting layer and is bent at a right angle (see FIG. 4B); and a buried conductor (110 or 210) filled in the groove-shaped via-hole.

Claim 26 is typically shown in FIGS. 5 and 6. The claim recitations correspond to the reference numerals as follows:

26. A semiconductor device according to claim 1, further comprising: a second interconnection (82) formed on the second insulating film (62) and formed of a conductor which is mainly formed of aluminum.

Claim 28 is typically shown in FIG. 6. The claim recitations correspond to the reference numerals as follows:

28. A semiconductor device according to claim 26, wherein the first interconnection (58) and the second interconnection (82) have the same pattern.

Claims 24, 31, 34 and 37 recite materials, which cannot be shown in the drawings.

Thus, the drawings show every feature recited in the claims which can be shown in the drawings.

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**Rejection Under 35 USC § 112, Second Paragraph:**

**Claims 1, 8, 10, 12, 20, 22, 25, 26, 28, 31, 34 and 37 were rejected under 35 USC § 112, second paragraph, as being indefinite.**

Claims 1, 22, 34 and 37 have been amended to further clarify the claims.

The structure of the claim 1 is shown in, e.g., FIGS. 4B and 6, as described above.

Claim 22 is rewritten into independent form in order to clarify the relationship between claim 1 and claim 22.

Claim 34 has been divided into two claims 34 and 41, and claim 37 has been divided into two claims 37 and 43.

Claims 8, 10, 12, 20, 25, 26, 28 and 31, depending from above claims, were rejected because of indefiniteness of the above claims, which has been overcome as shown above.

Therefore, the 35 USC § 112, second paragraph rejection should be withdrawn.

**Rejection Under 35 USC § 102(e):**

**Claims 1, 8, 10, 12, 20, 22, 24, 26, 28, 31, 34 and 37 were rejected under 35 USC § 102(e) as being anticipated by Shigeru et al. (JP 2001-351920).**

The Examiner alleged that Shigeru et al. discloses, in FIG. 1, a semiconductor device comprising: a first insulating film 11 formed over a substrate 1; a first interconnection 16 buried in at least a surface side of the first insulating film; a second insulating film 15 formed on the first insulating film with the first interconnection buried in, and including a groove-shaped via-

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hole 17 having a pattern which is bent at a right angle formed in a region above the first interconnection and a first buried conductor filled in the groove-shaped via-hole.

Element 16 of Shigeru et al., however, does not have a pattern which is bent at a right angle. Thus, element 16 of Shigeru et al. does not correspond to the first interconnection recited in claim 1 or the conducting layer recited in claim 22. Also, element 17 of Shigeru et al. is not a via-hole but a interconnection groove. The term "via-hole," means, in the relevant art, a hole for the electrical connection between two interconnection layers formed on different levels from each other. Element 17 of Shigeru et al. is not formed along an extending direction of the lower-level interconnection. Thus, Shigeru et al. does not teach or suggest the groove-shaped via-hole of the present invention. Therefore, claims 1 and 22 patentably distinguish over Shigeru et al. Claims 8, 10, 12, 20, 24, 26, 28, 31 and 37, directly or indirectly depending from claim 1, also patentably distinguish over Shigeru et al. for at least the same reasons.

Thus, under 35 USC § 102(e) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

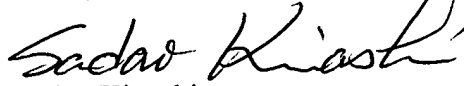
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If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

**WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP**



Sadao Kinashi

Attorney for Applicants  
Registration No. 48,075  
Telephone: (202) 822-1100  
Facsimile: (202) 822-1111

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